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Web

Results **1 - 10** of about **1,090,000** for <u>interrupt</u> <u>table</u> implementations. (0.12 seconds)

Operating System design & **implementation** Tutorial, planning a ...
Operating System Design & **Implementation** Tutorial - JOSH ... The second 'MOV'
command moves the CS value to the **Interrupt table** (remember that the current ...
www.mohanraj.info/josh5.jsp - 11k - <u>Cached</u> - <u>Similar pages</u>

4.1.9.1 **Interrupt** delivering
#include <hw/mdep/mEventTbl.h> // Exported interface <Off machine dependent event
table implementation dependencies. > <Off machine dependent **interrupt** ...
srg.cs.uiuc.edu/2k/off++/html/node88.html - 73k - <u>Cached</u> - <u>Similar pages</u>

Async **Interrupt** Block **Implementation** :: Asynchronous Support (Real ...
Async **Interrupt** Block **Implementation**. The source files for the Async ... and offset is an
interrupt table offset defined in the VME **interrupt** vector ...
www.mathworks.com/access/helpdesk/help/toolbox/rtw/ug/f24730.html - 13k -
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Package: eCos kernel
The **table implementation** involves a very small risk of overflow at run-time if a given
interrupt source is able to have more than one pending DSR. ...
ecos.sourceware.org/docs-1.1/ref/ecos-ref/package-cygpkg-kernel.html - 8k -
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[PDF] Design and **implementation** of **interrupt** packaging mechanism ...
File Format: PDF/Adobe Acrobat
Implementation and Environment. We implemented IPM in. Tender. , and applied IPM. to
interrupts from a Myrinet NIC. We assume that the. **Table** 2. ...
ieeexplore.ieee.org/iel5/8040/22210/01035023.pdf?arnumber=1035023 - <u>Similar pages</u>

An **Implementation** of User-level Restartable Atomic Sequences on ...
This paper outlines an **implementation** of restartable atomic sequences on the ... atomic
sequence since **interrupts** are dispatched via an **interrupt table**. ...
www.usenix.org/events/usenix03/tech/
freenix03/full_papers/mcgarry/mcgarry_html/index.html - 57k - <u>Cached</u> - <u>Similar pages</u>

Interrupts and Exceptions
The IDT is somewhat different from the **interrupt** vector **table** that exists in ... More
information about the **implementation** of **interrupts** and exceptions in ...
www.internals.com/articles/protmode/interrupts.htm - 21k - <u>Cached</u> - <u>Similar pages</u>

Analog Devices : Embedded Processing & DSP : Technical Support ...
The current **implementation** of VDK C/C++ ISR support on SHARC does take all the
required steps when entering and exiting **interrupts**. On SHARC an **interrupt** ...
www.analog.com/processors/cda/epTASearchResult/0,3001,,00.html - 961k -
<u>Cached</u> - <u>Similar pages</u>

[PDF] Software DMA **Implementation** Application Note
File Format: PDF/Adobe Acrobat - <u>View as HTML</u>
The DMA Channel **implementation** copies the number of packets (4 words) defined by
the ... FIQ **Interrupt**. **Table** 7. DMA Channel. Parameter. Value. Code Size ...
www.atmel.com/dyn/resources/prod_documents/DOC1169.PDF - <u>Similar pages</u>

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tree interrupt table   [Search]

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All Results

M Degermark

A Brodnik

J Mauro

D Gubb

A Ruiz

Method of scheduling interrupts to the linked lists of transfer descriptors scheduled at intervals ... - group of 3 »
DR Wooten - US Patent 5,832,492, 1998 - Google Patents
... In this manner a **tree** structure can be developed ... **TABLE** 2-continued Transfer Descriptor
Fields Name R/W ... INTO RThis field contains the **interrupt** delay count for ...
Cited by 20 - Related Articles - Web Search

... system using complete prefix **tree**, bit vector, and pointers in a routing **table** for determining where ... - group of 3 »
A Brodnik, M Degermark, S Carlsson, S Pink - US Patent 6,266,706, 2001 - Google Patents
... The forwarding **table** is essentially a **tree** with three levels. ... However, it is not necessary to actually build the prefix **tree** to build the forwarding **table**. ...
Cited by 23 - Related Articles - Web Search

[BOOK] Solaris Internals: Core Kernel Architecture - group of 3 »
J Mauro, R McDougall - 2000 - books.google.com
... **Tree** 25 Figure 2.1 Switching into Kernel Mode via System Calls 28 Figure 2.2 Process, **Interrupt**, and Kernel Threads 31 Figure 2.3 UltraSPARC I & II Trap **Table** ...
Cited by 54 - Related Articles - Web Search - Library Search

The balance between isoforms of the Prickle LIM domain protein is critical for planar polarity in ... - group of 8 »
... D Huen, D Coulson, G Johnson, D **Tree**, S Collier, J ... - Genes & Development, 1999 - Cold Spring Harbor Lab
... David Huen, Darin Coulson, Glynnis Johnson, David **Tree**, Simon Collier, and ... map to the proximal region and **interrupt** the 5 ... is 3' to the pkM 5' exon (**Table** 1) but ...
Cited by 77 - Related Articles - Web Search - BL Direct

Binary **tree** parallel processor - group of 2 »
SJ Stolfo, DP Miranker - US Patent 4,860,201, 1989 - Google Patents
... [45] Date of Patent: Stolfo et al. [54] BINARY **TREE** PARALLEL PROCESSOR [75] Inventors:
Salvatore J. Stolfo, Ridgewood, NJ; Daniel P. Miranker, Austin, Tex. ...
Cited by 68 - Related Articles - Web Search

TNet: a reliable system area network - group of 9 »
RW Horst, TC Inc, CA Cupertino - Micro, IEEE, 1995 - ieeexplore.ieee.org
... **Table** 1. Command and data symbol encoding. ... Designing for short latency imposes requirements such as short packet sizes and efficient **interrupt** handling. ...
Cited by 149 - Related Articles - Web Search - BL Direct

Method and apparatus for object-oriented **interrupt** system
T Saulpaugh, GK Slaughter, SK Bopardikar, X Zheng - US Patent 6,615,342, 2003 - patentstorm.us
... Issued on: October 21, 1997 Inventor: Ross 6308247 Page **table** entry management ... an entry for each **interrupt** source, arranged as an **Interrupt** Source **Tree**. ...

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(set OR enable) status interrupt

[Search Patents]

Patents

Patents **1 - 10** on **(set OR enable) status interrupt**. (0.21 seconds)

Buffered asynchronous communications element with receive/transmit control and status reporting
US Pat. 5241660 - Filed May 17, 1991 - National Semiconductor Corporation
Bit 3 of **Interrupt Enable** Register 32 enables the Modem **Status interrupt** when
set to logic 1. Bits 4 through 7 of **Interrupt Enable** Register 32 are always ...

Buffered asynchronous communications elements with receive/transmit control and status reporting
US Pat. 5287458 - Filed Mar 26, 1993 - National Semiconductor Corporation
Bit 0 indicates that the CTS Modem **Status interrupt** when **set** to logic 1. 40 Bit *
of Modem **Status** Register 46 is the Delta Data Bit 3 of **Interrupt Enable** ...

Packet-at-a-time reporting in a data link controller
US Pat. 4852088 - Filed Apr 3, 1987 - Advanced Micro Devices, Inc.
If the **status** regis-ter bit is **set** to ONE and either **interrupt enable** level is
not enabled, no **interrupt** is generated and the **Interrupt** Source Register bit ...

Microcomputer having separate access to complete microcode words and partial microcode words
US Pat. 4495563 - Filed Jul 2, 1981 - Texas Instruments Incorporated
EINT: **ENABLE** INTERRUPTS Opcode: 00000101 Definition: **Set** the **interrupt enable**
flag in the **status** thus enabling interrupts. **Set status** bit I to M'. ...

Microcomputer device using dispatch addressing of control ROM
US Pat. 4432052 - Filed Apr 13, 1981 - Texas Instruments Incorporated
EINT: **ENABLE** INTERRUPTS Opcode: 00000101 Definition. **Set** the **interrupt enable**
flag in the **status** thus enabling interrupts. **Set status** bit I to T. C, N, ...

Multiprogrammable input/output circuitry
US Pat. 4435763 - Filed Apr 13, 1981 - Texas Instruments Incorporated
Definition: **Set** the **interrupt enable** flag in the **status** thus enabling interrupts.
Set status bit I to T. C, N, A **set** to T. Applications: EINT is used to ...

Self-emulator microcomputer
US Pat. 4441154 - Filed Apr 13, 1981 - Texas Instruments Incorporated
The programmer assures that the **interrupt enable status** bit (and individual ...
Set status bit C to T. N is **set** to 'O1. Z is **set** to T. Applications: SETC is ...

Microcomputer having read/write memory for combined macrocode and microcode storage
US Pat. 4651275 - Filed Sep 26, 1984 - Texas Instruments Incorporated
The programmer assures that the **interrupt enable status** bit (and individual
interrupt enable bits in the I/O control register) are **set** before executing the ...

Servicing of interrupts with stored and restored flags
US Pat. 6493781 - Filed Aug 19, 1999 - Koninklijke Philips Electronics N.V.
The end of the nested second subroutine can include an **enable interrupt** ...

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(function OR channel) level interrupt (tree OR ¦   [Search Patents]

Patents   Patents 1 - 10 on (function OR channel) level interrupt (tree OR hierarchy). (0.09 seconds)

Method and apparatus for object-oriented interrupt system
US Pat. 6615342 - Filed Mar 27, 2000 - Sun Microsystems, Inc.
Sub-classes override this dummy method. This is set to the address of the native
first level Interrupt Handler function using the ...

Hierarchical apparatus and method for processing device interrupts in a computer system
US Pat. 5630141 - Filed Mar 7, 1996 - Taligent, Inc.
An apparatus for providing interrupt processing as can appear on more than one
level of said software hierarchy recited in claim 1, including processing ...

Interpretive digital data processor comprised of a multi-level hierarchy of processors and having program protection means
US Pat. 4346436 - Filed May 3, 1979 - Burroughs Corporation
There is a priority hierarchy for all interrupts. At any moment in time, operation
will be occurring at some interrupt (priorty) level and no lower priority ...

Microprocessor interface apparatus having a boot address relocator, a request pipeline, a prefetch queue, and an interrupt filter
US Pat. 5539890 - Filed Apr 21, 1995 - Tandem Computers Incorporated
8 shows an example of a three level interrupt hierarchy. ... and the check lines
carry check signals which are a function of the values on the information ...

Integrated hardware and software task control executive
US Pat. 6061709 - Filed Jul 31, 1998 - Integrated Systems Design Center, Inc.
13 and 14 illustrate some of the advantages of the interrupt hierarchy. ...
The interrupt exit function decrements the nest counter when the interrupt exits ...

Pipelined interpretive digital data processor comprised of a multi-level hierarchy of processors
US Pat. 4346435 - Filed Mar 23, 1979 - Burroughs Corporation
There is a priority hierarchy for all interrupts. At any moment in time, operation
will be 55 occurring at some interrupt (priority) level and no lower ...

Apparatus for dispatching data of the highest priority process having the highest priority channel to a processor
US Pat. 4028664 - Filed Mar 26, 1975 - Honeywell Information Systems, Inc.
Accordingly the priority tree 315 processor Pt has been selected in which ...
If there is a highest level interrupt (ie a ceive control of the processor. ...

Scalable tree structured high speed input/output subsystem architecture
US Pat. 5687388 - Filed Dec 8, 1992 - Compaq Computer Corporation
The sender samples its instance, if a level 15 interrupt causes the PIC 108 to
assert CTS ... request the current sender to reverse the channel at the end.

Processor interface chip for dual-microprocessor processor system
US Pat. 6397315 - Filed Apr 21, 1995 - Compaq Computer Corporation
8 shows an example of a three level interrupt hierarchy. ... and the check lines

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"status register" interrupt

Search Patents

Patents

Patents **1 - 10** on **"status register" interrupt**. (0.29 seconds)

Data transfer control circuit with **interrupt status register**
US Pat. 6883053 - Filed Oct 12, 2001 - Oki Electric Industry Co., Ltd.
One of the data receiver-transmitters has an **interrupt status register** with bits
indicating the logic levels of the **interrupt** signals from each of the data ...

Interrupt status register for interface adaptor chip
US Pat. 4069510 - Filed May 24, 1976 - Motorola, Inc.
[54] **INTERRUPT STATUS REGISTER** FOR INTERFACE ADAPTOR CHIP [75] Inventors: Earl F.
Carlow, Scottsdale; Michael F. Wiles, Phoenix, both of Ariz. ...

System for determining adapter **interrupt status** where **interrupt** is sent to host after operating **status** stored in **register** is shadowed to host memory
US Pat. 6078970 - Filed Oct 15, 1997 - International Business Machines Corporation
The device **interrupt status register** stores the **interrupt** status of the I/O adapter.
The I/O adapter accesses the **interrupt** status shadow address register ...

Transformation of a first dataword received from a FIFO into an input **register** and subsequent dataword from the FIFO into a normalized output dataword
US Pat. 6061749 - Filed Feb 18, 1998 - Canon Kabushiki Kaisha
... bits Status DCC error **status register** Controll DCC error **interrupt** enable ...
Status **Status Register Interrupt** Error/**Interrupt Status Register** Config2 ...

Buffered asynchronous communications element with receive/transmit control and **status** reporting
US Pat. 5241660 - Filed May 17, 1991 - National Semiconductor Corporation
... (LS) DIVISOR LATCH (MS) UNE **STATUS REGISTER** TRANSMITTER HOLDING REGISTER ...
MODEM STATUS M REGISTER **INTERRUPT** ENABLE REGISTER **INTERRUPT** ID REGISTER ...

Method, apparatus and system for managing virtual memory with virtual-physical mapping
US Pat. 6336180 - Filed Feb 18, 1998 - Canon Kabushiki Kaisha
... bits Status DCC error **status register** Controll DCC error **interrupt** enable ...
Status **Status Register Interrupt** Error/**Interrupt Status Register** Config2 ...

Memory controller architecture
US Pat. 6118724 - Filed Feb 18, 1998 - Canon Kabushiki Kaisha
... Register Status **Status Register Interrupt** Error/**Interrupt Status Register**
Config2 Error/**Interrupt** Enable Register Config2 Data Manipulation Register ...

System for managing input/output accesses at a bridge/memory controller having a **status register** for recording cause of **interrupt**
US Pat. 6298399 - Filed Jan 31, 2000 - Intel Corporation
... **status register** ... **interrupt** ...

General image processor
US Pat. 6289138 - Filed Feb 18, 1998 - Canon Kabushiki Kaisha
... Registers Config2 Configuration Register Status **Status Register Interrupt**